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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/818,906	03/28/2001	Keiichiro Wakamiya	50090-290	2402

7590 09/10/2004

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EXAMINER	
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ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/10/2004

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/818,906
Filing Date: March 28, 2001
Appellant(s): WAKAMIYA, Keiichiro, et al.

Arthur Steiner
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 06-22-04.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences, which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief has been changed as follows:

I. Claims 1-6 are allowed.

Reasons for allowance

The references of record do not teach either singularly or in combination at least the limitations "wherein the connecting conductor includes a plurality of layers formed of same material and at least one of the layers is formed as a stress-absorbing layer having lower hardness than other layer" in a device having a plurality of connecting conductors penetrating through a coating layer and being connected to a surface of a chip and to external terminals beyond an outside surface of the coating layer.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-13 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of the claims under appeal.

6,159,837	Yamaji et al.	12-2000
6,181,569	Chakravorty	01-2001
5,952,718	Ohtsuka et al.	09-1999
5,886,415	Akagawa	03-1999
6,436,802	Khoury	08-2002

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

I. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

II. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (US Pat. 6159837) in view of Chakravorty (US Pat. 6181569) and Ohtsuka et al. (US Pat. 5952718).

Regarding claims 7 and 8, Yamaji et al. disclose a semiconductor device comprising:

- a semiconductor chip/wafer (1 in Fig. 3)
- a plurality of protective insulating layers (3/5 in Fig. 3) comprising a protective coating/film (3 in Fig. 3; Col. 5, line 46) covering the surface of the chip/wafer

- a plurality of connecting conductors including a plurality of stacked layers and an electrode lead (4a and 7 in Fig. 3) connected to the surface of the chip/wafer and penetrating the coating layer beyond the outside surface of the coating layer, wherein the connecting conductors are connected to bumps as external terminals (8 in Fig. 3) beyond the outside surface of the coating layer
- the connecting conductors do not include wiring layers and bumps (Fig. 3; Col. 7, lines 23-40) and the connecting conductors including a plurality of connecting conductors (38/31 and 38'/31), and
- the connecting conductors including the plurality of layers formed of different metals comprising the stacking of barrier metals including titanium, nickel and palladium (col. 7, line 24; Col. 5, line 52) and a solder (7 in Fig. 3; Col. 7, line 11; Col. 7, line 46)

(Fig. 3; Col. 7, lines 20-47; Col. 5-7).

Yamaji et al. fail to teach the plurality of layers of the connecting conductors being formed of different material where at least one of the connecting conductor layers being formed as a stress-absorbing layer having lower hardness than the other layer.

Chakravorty teaches a device (see Fig. 10g) having a plurality of the connecting conductors being connected to a bump as an external terminal where the connecting conductors include an under bump metallization (UBM) having a combination/stacking

of chromium (Cr) and copper (Cu) metal layers (321 in Fig. 10b-10g; Col. 9, line 26) and a conductor layer (325 in Fig. 10f and 10g; Col. 14, line 9) being connected to a pad on a chip (304 and 302 respectively in Fig. 10a-10g). Furthermore, one of the plurality of layers (325 in Fig. 10f and 10g) is formed from a metallic material as that of the UBM layers or a different material such as non-metallic/conductive polymer material (Col. 14, lines 20-30; Col. 13, line 25- Col. 14, line 35).

Ohtsuka et al. teach using a plurality of conducting barrier layers/conductors (35/38/36 in Fig. 3-5c) in a device to reduce mechanical stress in a device where one of the layers is made of stress absorbing layer such as gold (38 in Fig. 5b/5c), the gold having a lower hardness (Col. 5, line 62) than that of the other connecting conductor layer such as nickel (35 in Fig. 5b/5c- see hardness values of about 30-40 Hv for gold as compared to about 450-500 Hv for nickel in Col. 5, lines 49-62).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the plurality of layers of the connecting conductors being formed of different material as taught by Chakravorty and at least one of the connecting conductor layers being formed as a stress absorbing layer having lower hardness than the other layer as taught by Ohtsuka et al. so that the mechanical stress and chip cracking defects can be reduced and the desired hardness and bonding strength can be achieved in Yamaji et al's device.

III. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (US Pat. 6159837), Chakravorty (US Pat. 6181569) and Ohtsuka et al. (US Pat. 5952718) as applied to claim 7 above, and further in view of Akagawa (US Pat. 5886415).

Regarding claims 9 and 10, Yamaji et al., Chakravorty and Ohtsuka et al. teach substantially the entire claimed structure as applied to claim 7 above, except the connecting conductor being formed from an anisotropic conductive material or a conductive material containing metal particles respectively.

Akagawa teaches a semiconductor device having connecting conductors connected to a chip surface/electrode (36 in Fig. 2, 3, 7 and 8) where the connecting conductors are formed of an anisotropic conductive material (38 in Fig. 2, 3, 7 and 8; Col. 4, lines 10-25) containing metal particles (39 in Fig. 2, 3, 7 and 8; Col. 1, line 40), the anisotropic conductive material being of low hardness and being functional as a shock absorbing layer to protect the chip/device (Col. 8, lines 1-5; Col. 10, lines 30-35).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the connecting conductor being formed from an anisotropic conductive material or a conductive material containing metal particles as taught by Akagawa so that the mechanical stress and chip cracking defects can be reduced and bonding can be improved in Chakravorty, Ohtsuka et al. and Yamaji et al's device.

IV. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (US Pat. 6159837), Chakravorty (US Pat. 6181569) and Ohtsuka et al. (US Pat. 5952718) as applied to claim 7 above, and further in view of Khoury (US Pat. 6436802).

Regarding claims 11-13, Yamaji et al., Chakravorty and Ohtsuka et al. teach substantially the entire claimed structure as applied to claim 7 above, wherein Ohtsuka et al. further teach the connecting conductors being of substantially identical diameter (see 35/36/38 in Fig. 5c), but Yamaji et al., Chakravorty and Ohtsuka et al. fail to teach forming the connecting conductors by stacking a plurality of layers in a staggered manner, the plurality of layers of the connecting conductors being of different diameter from each other in the sequence of layers respectively.

Khoury teaches forming a contactor (230 in Fig. 7A-7L) having a plurality of metal conductors/layers such as aluminum, copper, nickel, etc. on a pad/trace (232 in Fig. 7A-7L) where the plurality of metal layers are stacked in a staggered manner, the plurality of layers of the connecting conductors being of different width (W)/diameter (D) from each other in the sequence of layers respectively (see W/D of the conductors in 237, 242, 243, etc. in Fig. 7L) to expand/fan-out pitch of the contactors and external contacts (Col. 8, lines 53- Col. 9, line 60; Col. 7, line 10- Col. 8, line 10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the connecting conductors by stacking a plurality of

layers in a staggered manner, the plurality of layers of the connecting conductors being of substantially identical diameter or different diameter from each other in the sequence of layers respectively as taught by Ohtsuka et al. and Khoury so that the desired spacing/pitch for the external contacts can be achieved and the bonding strength can be improved in Chakravorty, Ohtsuka et al. and Yamaji et al's device.

(11) Response to Arguments

I. Rejection of claims 7 and 8:

A. Appellant argues that the barrier metal 4a in Yamaji et al. is a "lead pattern" and is a part of a wiring layer (Col. 7, line 56) and therefore, is not a connecting conductor.

However, Yamaji et al. (see Fig. 3 of Embodiment 2; Col. 7, lines 20-42) clearly teach forming the barrier metal/conductor on the pad of the chip (see 4a and 2 respectively in Fig. 3) such that a lead pattern is not formed to improve reliability and electrical performance of the device (see Col. 7, line 23 and lines 37-42). It seems that appellant's remarks (Col. 7, line 56) are made in reference to another embodiment (see Fig. 4 of Embodiment 3; Col. 7, line 56) and therefore, are not applicable to the above rejections.

B. Appellant argues that Ohtsuka et al. disclose the wiring layers/diffusion barriers and not the connecting conductors as claimed and furthermore, the diffusion barriers do not protrude from the protective layer 34 in Fig. 3.

However, Ohtsuka et al. clearly show in Fig. 3-5c, the plurality of conductive barrier layers/conductors (see 35, 38 and 36 in Fig. 3-5C) being connected to the chip electrode (33 in Fig. 3-5c) and a protruding contact (37 in Fig. 3-5c), the chip electrode being further connected to an active layer within the chip including wiring, contacts, etc. (Col. 3, lines 6-10 and 15-55). Therefore, of conductive barrier layers/conductors in Ohtsuka et al. are the connecting conductors, which connect the chip electrode and the protruding contact.

Furthermore, the primary reference of Yamaji et al. teach the structure comprising the coating layer such that the connecting conductors penetrate the coating layer beyond the outside surface of the coating layer. Ohtsuka et al. is combined with Yamaji et al., because Ohtsuka et al. teach using the conductor layers of different material having different hardness.

C. Appellant argues that Ohtsuka et al. teach away from the invention by forming the diffusion barriers within the protective layer (layer 34 in Fig. 3).

However, the invention also discloses the connecting conductors/post (see 4 in Fig. 1-3) being formed entirely within the protective insulating layer made of the sealing

resin and the coating layer (see 5 and 7 in Fig. 1-3; see specification page 5, lines 25-28; page 7, lines 2-6). Examiner holds that Ohtsuka et al. do not teach away from the invention by forming the connecting conductors being protected by the insulating layer.

II. Rejection of claims 9 and 10:

Appellant did not present any new arguments regarding claims 9 and 10.

III. Rejection of claims 11-13:

Appellant did not present any new arguments regarding claims 11-13.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

NP
September 2, 2004

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